Nanophotonic Devices for Power-efficient Computing and Optical Interconnects

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Abstract

To solve the problem in huge power consumption of the data centers and cloud computing, we design an extreme optical adder architecture suitable for ultra-high bit count. n-bit full adder are full implementable on a silicon platform using guided wave optics.

Even if the continuation of Moore's law meets a bottleneck, the increasing trend of network connections and bandwidth consumed is accelerating with no foreseeable sign of halting because of the bandwidth-hungry applications. The total amount of content passing through the world's networks is expected to increase to 35 Zettabytes（10^{21}）with unprecedented power consumption by 2020, meaning that by the end of this decade, with current technologies, service providers will need an astonishing over 20 times of power consumption they have in 2017.

Optoelectronic interconnects and optical logic gates provide key solutions to drastically reduce the power to modulate (e-to-o conversion), process, transport, and demodulate (o-to-e) high-speed signals with power consumption down to attojoule/bit (AJ/B) level[1]. In this invited paper, we propose a myriad of ultra-low power nano-optoelectronic devices for intra- and inter-chip optical interconnects [2] and computing. A vertical cavity surface emitting nano-lasers is proposed with high injection current confinement and extremely high quantum efficiency that can provide 1 to 2 orders magnitude power saving to 100 Gbit/sec. A modified uni-traveling carrier (MUTC) photo receiver is also proposed to solely utilize highly mobile electrons to provide o-to-e conversion with near-to-unity quantum efficiency at zero bias that can be integrated on a silicon photonics platform (Figure 1). An innovative modulator using the combination of the slow light effect on Si photonic crystal and the plasmonic free carrier absorption effect drastically reduces the device size and modulation efficiency to <100 AttoJoule/Bit level at above 25 Gbit/sec, which is at least one order of magnitude less than the state-of-the art devices. To provide wavelength routing in a WDM (wavelength division multiplexing) based on-chip network, a low power n x n wavelength router is proposed using 2D photonic crystal based slow light effect with great power saving capability[3].

To further solve the problem in huge power consumption of the state-of-the-art data centers and cloud computing, we propose to take advantage of the optical computing and design an extreme adder architecture suitable for ultra-high bit count (such as 64, 128, 256-bit) (Fig.2). Our proposed n-bit full adder are full implementable on a silicon platform using guided wave optics. Note that all the basic digital logic functions can be realized employing optical logic devices without energy consumption (0 joule/bit) while the calculation is being performed. Energy is only expended when the final result is being extracted. In electronics, energy is dissipated at each step along the calculation path. Another tremendous advantage over the conventional electronic scheme is the elimination of gate latency and simultaneous availability of a logic function and its complementary at the output, which makes the approach proposed herein extremely efficient. The proposed device implementation for a 256-bit carry-ripple adder is capable of providing two orders of magnitude

power saving and one order of magnitude of latency reduction (and therefore one order of magnitude faster in computing speed) when compared to the electronic counterparts.

In this paper, further simulation results for power-efficient full adders and optical interconnects will be presented with some experimental data.

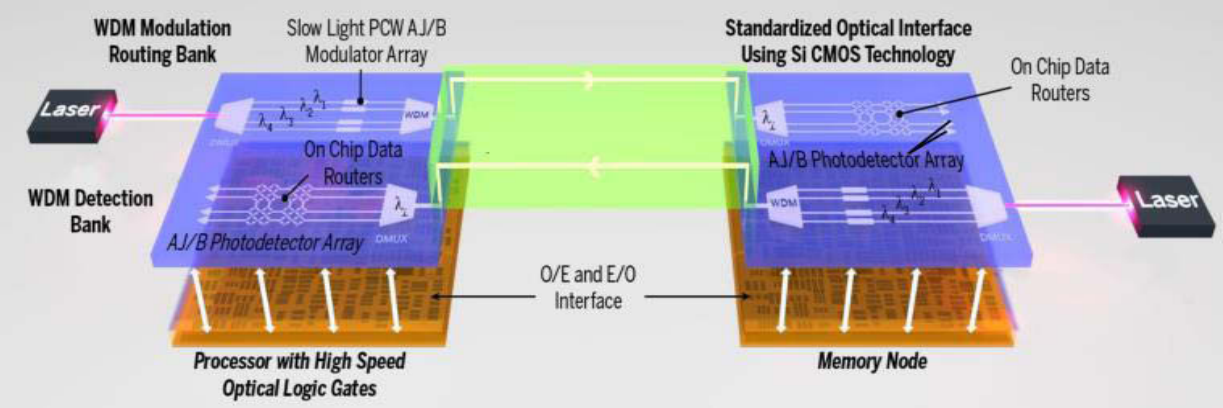

Figure 1 Schematic of the proposed power-efficient intra- and inter-chip optical computing & interconnects with all innovated active and passive devices on a silicon platform

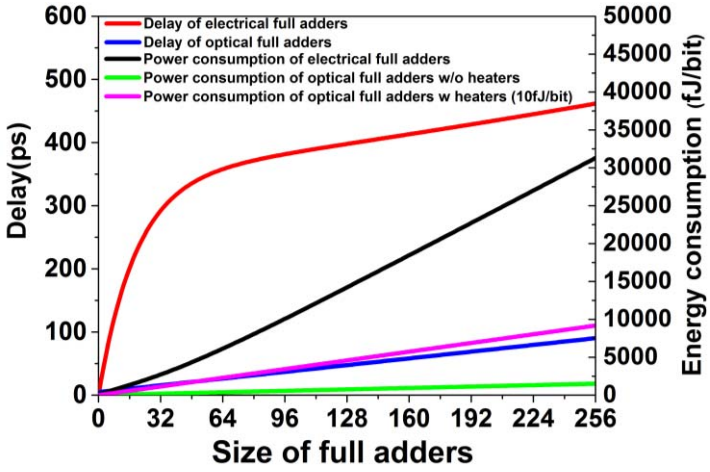

Figure 2 Comparison of the optical full adders with the electronic counterparts. Two key parameters under consideration are energy consumption and latency. The data quoted in this chart are from references [4,5]

References

1. David A. B. Miller, "Attojoule Optoelectronics for Low-Energy Information Processing and Communications: a Tutorial Review," *IEEE/OSA J. Lightwave Technology* 35 (3), 343-393 (2017)
2. R T Chen, L Lin, C Choi, YJ Liu, B Bihari, L Wu, S Tang, et al., "Fully embedded board-level guided-wave optoelectronic interconnects" *Proceedings of the IEEE*, pp. 780-793 2000
3. X Chen, YS Chen, Y Zhao, W Jiang, RT Chen, "Capacitor-embedded 0.54 pJ/bit silicon-slot photonic crystal waveguide modulator,"*Optics letters* 34 (5), 602-604, 2009
4. Timurdogan, E., Sorace-Agaskar, C.M., Sun, J., Hosseini, E.S., Biberman, A. and Watts, M.R., 2014. An ultralow power athermal silicon modulator. *Nature communications*, 5(2014).
5. Roy, S., Choudhury, M., Puri, R. and Pan, D.Z., Polynomial time algorithm for area and power efficient adder synthesis in high-performance designs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *35* (5), 2016.