Electro-Optic Ripple-Carry Adder in Integrated Silicon Photonics for Optical Computing

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***Abstract*—Photonic integrated circuits with compact size and low power consumption have opened the possibility of realization of ultrahigh-speed and energy-efficient optical computing in an integrated system that may be comparable to CMOS-based electrical integrated circuits in many aspects. Directed logic is an innovative paradigm that can make full use of the advantages of electronics and photonics for optical computing. In this paper, we propose various designs of directed-logic-based electro-optic ripple-carry adders in integrated silicon photonics, which replace the electrical components in the critical path using optical counterparts. All control signals are applied simultaneously through ultralow-power microdisk modulators so that the propagation delay could be reduced significantly. A two-bit thermal-optic full adder based on microdisk modulators is demonstrated as a proof of concept along with a projection of high-speed performance. The proposed electro-optic full adder paves the way to future low-power-consumption and large-bandwidth optical computing in integrated silicon photonics.**

***Index Terms*—Optical computing, optical logic devices, silicon on insulator technology, microresonators, electro-optic devices.**

I. Introduction

COMPLEMENTARY metal-oxide-semiconductor (CMOS) large scale integration (LSI) technologies have been making significant contributions to today's rapidly improving modern society with information explosion. However, as predicted, with the continuous downscaling of transistors and metal interconnects over the past five decades, the power consumption and transmission bandwidth have been approaching the unavoidable limitation [1], [2]. A new alternative technology is required to continue Moore's law and meet the drastically increasing bandwidth requirements. This has led to considerable academic and industrial research on silicon photonics in the past two decades due to its unique properties of low latency, low power consumption, and high bandwidth. In addition, it is also compatible with the CMOS fabrication line, leading to low fabrication cost.

With the development of silicon photonics, various mature passive and active building blocks have been demonstrated experimentally and have even become available as standard components with guaranteed performances in the libraries from foundries, including interconnects [3]–[5], electro-optic switches or modulators [6], [7], and photodetectors [8], which herald the next generation of revolutionary technologies and applications. Optical computing has attracted more and more attention these years as they have the potential to overcome the speed limitation intrinsic to electronics. Directed logic, which employs optical switch networks to realize logic operations, is regarded as an innovative paradigm for optical computing [9]. It makes full use of photonics and electronics and has been investigated by many researchers theoretically and experimentally since it was introduced in 2007. Various optical logic gates and modules based on directed logic, such as AND/NAND, OR/NOR gates [10], XOR/XNOR gates [11], [12], encoders [13], and half adders [14], have proved to own the potential to serve in a future high-speed optical computing system [15]–[19].

In this paper, we first introduce a new architecture in integrated silicon photonics based on directed logic that combines the merits of photonics and electronics for optical computing. After a summary of building blocks for directed logic, four designs of ripple-carry full adders are proposed and discussed based on different components. A selection of high-performance electro-optic (EO) modulators is then presented considering in many aspects such as the compactness and power consumption. Finally, a microdisk-based two-bit EO ripple-carry full adder is demonstrated experimentally as a proof of concept to show the feasibility of EO full adders with the projected high-speed performance discussed in the end.

II. Architecture of the Integrated EO Computing System

A. Architecture

Directed logic was first introduced in 2007 by Hardy and Shamir that employs optical switch networks to perform

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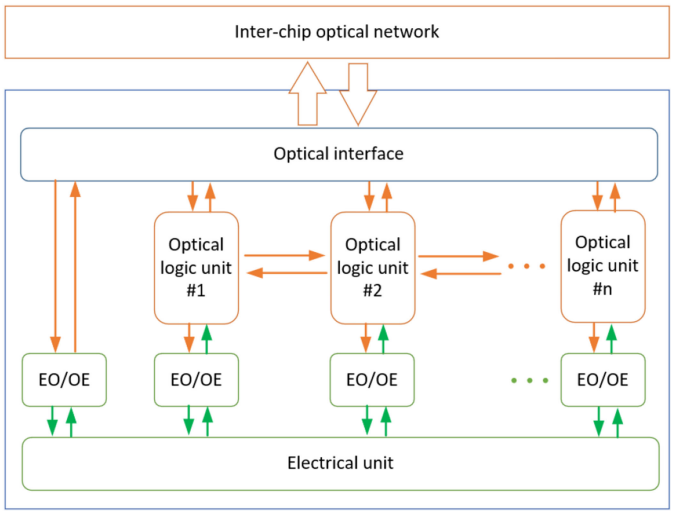

Fig. 1. Architecture of the proposed integrated EO computing system.

distributed parallel computation of a function and its negation [9]. All these optical switches are set by electrical signals simultaneously before the injection of light. The light beam will then go through all the paths defined by these modules and finally be detected by monitors to read out the results. One important feature of the directed logic is that the operation of each element is totally independent of the operations of the other elements in the circuit (i.e., no all-optical switches are needed in the circuits), and computation can only be performed by the circuit as a whole. Only under this condition the optimal computing speed can be achieved, otherwise one logic gate has to wait for the related signals to be calculated from previous stages and consequently the latency accumulates. Another reason that all-optical switches or modulators are not taken into consideration here is that all-optical components demonstrated up to date still need lots of power per bit which may not satisfy the requirement of low-power optical computing [20]. As is known, electrical parts have the advantages of convenience and flexibility of control while the optical parts could carry and deliver signals at speed of light. Directed logic combines these merits by using the electrical circuits to apply the operands and in the meantime using the photons to carry and process the information. Therefore, directed logic is a highly promising candidate for future high-speed and low-power-consumption optical computing in integrated silicon photonics.

In Fig. 1, we propose an architecture of the integrated EO computing system to implement the directed logic. Within this system, optical logic units play the most important role, which receive signals from adjacent units or the optical network through optical interfaces and also deliver the results to these destinations in the optical format without any OE/EO conversion or optical memories in between. The optical interface consists of optical routers, (de)multiplexers, combiners/splitters and so on. Each element is independent of each other as discussed above. The control signals are applied by the electrical units simultaneously followed by the injection of light at every clock cycle. At each optical logic unit, some light may be dropped off and be received by photodetectors to generate electrical results and then be processed or stored in the electrical units. Optical results may also directly return to the intra-chip optical network to communicate with other modules in a more efficient way. Electrical units are also able to talk to other chips through EO/OE conversion modules.

TABLE I
SEVERAL FUNDAMENTAL EO LOGIC GATES

Logic gate	Electrical input	Optical output	Expression
Inverter	a	A	$A = \lambda a$
		$\bar{A}$	$\bar{A} = \lambda \bar{a}$
OR/NOR	a, b	$A + B$	$A + B = \lambda(a + b)$
		$\overline{A + B}$	$\overline{A + B} = \lambda(\overline{a + b})$
AND/NAND	a, b	$A \cdot B$	$A \cdot B = \lambda(a \cdot b)$
		$\overline{A \cdot B}$	$\overline{A \cdot B} = \lambda(\overline{a \cdot b})$
XOR/XNOR	a, b	$A \oplus B$	$A \oplus B = \lambda(a \oplus b)$
		$\overline{A \oplus B}$	$\overline{A \oplus B} = \lambda(\overline{a \oplus b})$

B. Electro-Optic Logic Modules

Optical logic units are the key components to process the optical signals under the control of electrical inputs. This process can be expressed in a matrix format as:

$$N = TM, \tag{1}$$

where M is the input vector, N is the output vector, and T is the processing matrix of the optical logic unit. Examples will be presented hereinafter. The matrix T is mostly determined by the passive and active components in the module. EO modulators convert electrical signals into optical formats efficiently, making them essential for high-speed optical computing. Fortunately, high-performance EO modulators in silicon platform have been widely investigated and demonstrated by many research groups as well as many foundries [6], [21]–[24], making various logic functions accessible in the optical domain.

Some published EO logic gates are listed in Table I [10], [15]. λ means continuous wave input. It can be seen from the expressions that operations between electrical inputs are calculated first and the continuous wave will then map the calculated result to optical ones. Replacing λ with optical signals, for example, H, can lead to multiplication between electrical and optical operands, for example, $H \cdot (a + b)$. It should be noted that only multiplication out of all the operations can be done between signals from two different domains and all the outputs are in the optical domain, which also indicates that this computing process is irreversible without a photodetector. However, this results in a severe problem since there are no feasible operations that we can implement between two or more optical inputs if nonlinearity is not taken into consideration and consequently the applications would be narrowed down into a relatively small area.

Fortunately, in some special cases, an optical combiner can be used to mimic an optical logic gate. For example, a widely used optical combiner such as a multimode interferometer (MMI) or a Y-branch [25] has the capability of serving partially as an OR gate with a constraint condition that both arms cannot allow light to pass through simultaneously. Note that 3 dB insertion

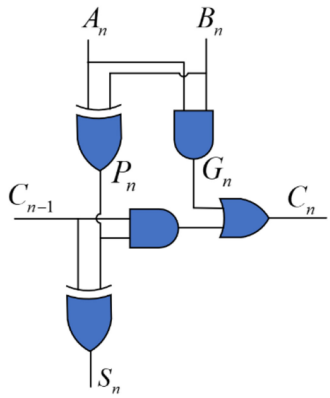

Fig. 2. Schematic of a one-bit conventional electrical full adder.

loss will be added unavoidably due to the mode imbalance of the two arms when only one has light going through.

III. Electro-Optic Ripple-Carry Adder

A. Electrical Full Adder

A one-bit full adder is a digital circuit that adds three one-bit binary numbers, two addends and one carry, and outputs two one-bit binary numbers, a sum and a carry. It is widely used in the arithmetic logic units (ALUs) as well as address and index calculators in many computers and other kinds of microprocessors, which usually functions as a component in a cascade of adders, adding 8, 16, 32, etc. binary numbers. For a one-bit adder, normally the two addends are written as A and B, and the carry input is denoted as C_{in}. C_{out} and S represent the carry and sum outputs, respectively. The expression for a full adder can be summarized by

$$C_n = (A_n \oplus B_n) \cdot C_{n-1} + A_n \cdot B_n = P_n \cdot C_{n-1} + G_n \quad (2)$$

$$S_n = C_{n-1} \oplus (A_n \oplus B_n) = C_{n-1} \oplus P_n \quad (3)$$

where $P_n = A_n \oplus B_n$ (propagate) and $G_n = A_n \cdot B_n$ (generate). Fig. 2 shows the logic diagram of a one-bit conventional electrical full adder. One can easily tile this block horizontally to realize N-bit full adders, which is called the ripple-carry adder since the carry signal C ripples to the next bit. However, waiting for the carry bit will incur a large delay. Specifically, the delay for a n-bit electrical full adder can be calculated by $t_e = t_{dr} + n \times t_{epb}$, where t_{epb} is the delay for each bit and t_{dr} is the time for generating P and G. All P and G signals can be generated simultaneously. In practice, t_{epb} is several picoseconds to tens of picoseconds [26], [27]. For a n-bit adder, the latency accumulates as *n* increases because of the serialization of the propagation delay, which leads to relatively larger latency.

On the contrary, as is known, photons travel much faster than electrons on a chip and are endowed with the immunity to the distributed capacitance and resistance. For example, light only need to spend around 0.14 ps to go through a 10 μm long silicon waveguide in a silicon-on-insulator (SOI) platform. It also allows the P and G signals to be applied to the modulators simultaneously within every clock cycle. The total delay for this EO full adder therefore can be calculated by $t_o = t_{dr} + t_{sw} + n \times t_{opb}$, where t_{dr} means the delay for generating P and G, t_{sw} means the switching time of the EO modulator, and t_{opb} is the propagation latency for each bit. Since $t_{opb} \ll t_{epb}$, the total latency of an EO full adder can be reduced drastically as the bit size increases.

B. 6M Design of an EO Full Adder

To design a high-speed full adder based on the directed logic with optimal performance, we first clarify the inputs and outputs of this optical logic unit. Here, we use electrical logic gates to generate P and Q first since this process is not involved in the critical path and all the P and Q signals could be generated simultaneously. This method is widely used in the very large scale integration (VLSI) design of full adders [28]. In this case, P and Q need to be regarded as the electrical inputs. For the carry signal C, it has to be in optical format since it is calculated from the previous bit and travels all the way to its destination along the critical path to deliver information. However, upon these assumptions, XOR operation between optical C and electrical P is not feasible, which means that the calculation of the sum based on (3) will not be ideal. Therefore, (3) needs to be rewritten as

$$S_n = C_{n-1} \cdot \overline{P_n} + \overline{C_{n-1}} \cdot P_n, \quad (4)$$

at the cost of calculating extra $\overline{C_n}$, which could be calculated by

$$\overline{C_n} = \overline{C_{n-1}} \cdot \overline{G_n} + \overline{K_n}, \quad (5)$$

where $K_n = A_n + B_n$. A matrix transmission can easily conclude the whole calculation process, which is

$$\begin{pmatrix} C \\ S \\ \lambda \\ \bar{C} \end{pmatrix}_n = \begin{pmatrix} P_n & 0 & G_n & 0 \\ \bar{P}_n & 0 & 0 & P_n \\ 0 & 0 & 1 & 0 \\ 0 & 0 & \bar{K} & P_n \end{pmatrix} \cdot \begin{pmatrix} C \\ S \\ \lambda \\ \bar{C} \end{pmatrix}_{n-1}, \quad (6)$$

which includes the optical input vector M_{n-1}, the optical output vector M_n and the electrical transformation matrix T_n, consistent with (1). This equation is also highly scalable, for instance, in an N-bit system, the equation becomes

$$M_n = T_n \cdot T_{n-1} \ldots T_1 M_0. \quad (7)$$

Finally, a six-modulator (6M) design can be drawn based on (2), (4), and (5), as shown in Fig. 3(a), where the applied electrical signals for six resonators $(a$–$f)$ are P_n, G_n, $\overline{K_n}$, $\overline{G_n}$, $\overline{P_n}$, and P_n, respectively. All kinds of EO modulators could be candidates in this design and here we choose microresonators as an example to illustrate the working principle. For a resonator-based modulator, the applied voltage changes the refractive index of the cavity through carrier dispersion effect or thermal-optic effect [23], [29] and then the spectrum shifts, as shown in Fig. 3(b). In the figure, if the working wavelength is set at λ_1, a direct digital signal mapping from electrical domain to optical domain is observed. On the contrary, for the wavelength λ_2, a logic negation appears at the optical output. For a dual-bus resonator, the optical signals and the logic negation could be obtained at two ports at the same time. Here, for simplicity,

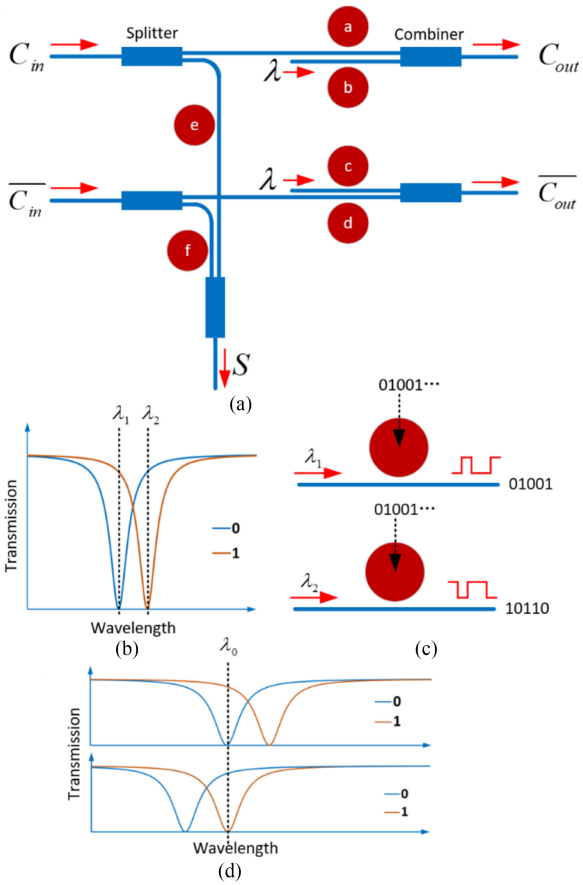

Fig. 3. (a) The 6M design of an EO full adder. (b) The spectrum shift at different voltage supplies. (c) The digital output for different working wavelengths. (d) Two resonators are aligned to share one working wavelength but at different voltage supplies.

we choose resonators with the well-aligned spectra like the one shown in Fig. 3(d), which can be achieved by choosing different sizes or thermal tuning, and then set the source wavelength at λ_0. Therefore, only one electrical signal is required for each pair and specifically only P_n, G_n, and K_n should be provided in this case.

C. 4M Design of an EO Full Adder

Directed logic circuits prefer to perform distributed parallel computing of a function as well as its negation simultaneously by a vector operation-based computing method. Using a pair of these results, a function and its inverse, at the same time sometimes makes the design more compact, saves more active components, and consequently reduces power consumption. For example, in the design of full adders, if a dual-bus modulator is adopted to generate logic pairs, only four modulators are required as shown in Fig. 4(a). In order to illustrate the four-modulator (4M) design clearly, we need to rewrite (2) and (5) as

$$C_n = C_{n-1} \cdot P_n \cdot \overline{G_n} + \lambda \cdot G_n, \tag{8}$$

$$\overline{C_n} = \overline{C_{n-1}} \cdot P_n + \lambda \cdot \overline{K_n}. \tag{9}$$

These equations are logically equivalent to the original ones and can be deduced using formula $a + b = a \cdot \bar{b} + b$ along with

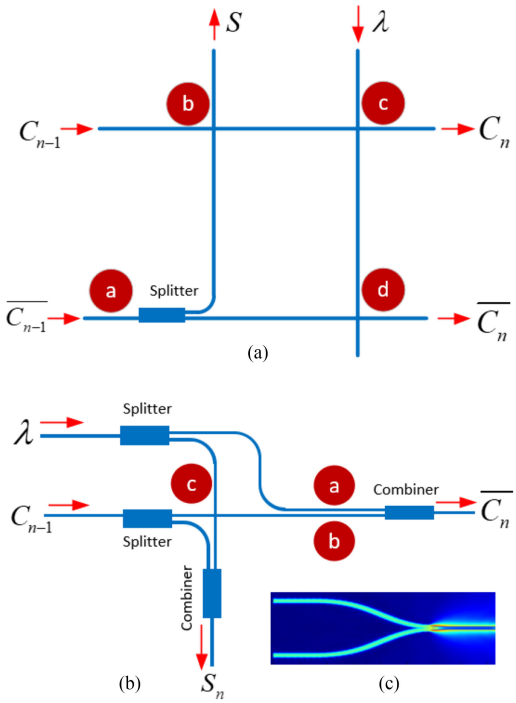

Fig. 4. (a) The 4M design and (b) the 3M design of an EO full adder. (c) The mode profile of a combiner when coherent light beams at two arms have π phase difference.

TABLE II
TRUTH TABLE OF AN OPTICAL XOR GATE

1st arm input	2nd arm input	Phase difference	Intensity	XOR gate
0	0		0	0
0	1		0.5	1
1	0		0.5	1
1	1	π	0	0
1	1	0	2	

$\overline{G_n} \cdot K_n = P_n$. When the wavelength λ_1 is chosen as the light source as depicted in Fig. 3(c), the electrical signals $(a$–$d)$ are P_n, P_n, $\overline{G_n}$, and $\overline{K_n}$, respectively. Otherwise, they should be their negations. Now one can directly map the design to the equations easily.

D. 3M Design of an EO Full Adder

Due to the limited operations between optical signals, (3) needs to be expanded to (4) and (5). However, there is one exception that the XOR gate actually has its corresponding optical substitute. An optical combiner could be one of the candidates to mimic the XOR gate using optical interference since the state of (1,1) with the output of 0 can be perfectly achieved by the destructive interference, which is a unique property of photons in contrast to electrons. As shown in Table II, when light only exists in one arm, the output will be half of the input intensity due to the mode mismatch, which could be defined as logic 1 but with 3 dB insertion loss. For the case that two inputs go through the combiner together, the output highly depends on the phase difference. Exact π phase difference will generate a total destructive interference to cancel out each other and finally logic 0 is achieved as shown in Fig. 4(c). As can be seen, the

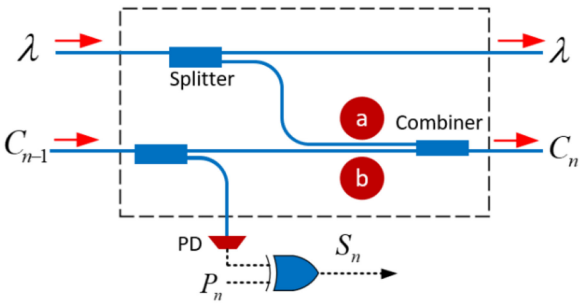

Fig. 5. The 2M design of an EO full adder with only two EO modulators. a: G_n signal. b: P_n signal.

first four states in Table II match well with the truth table of an XOR gate as long as the phases of the two arms are fine-tuned so that the fifth state in the table or other states will not emerge unexpectedly. The 4M design is presented in Fig. 4(b). The electrical signals for modulators (*a*–*c*) are G_n, P_n, and P_n, respectively when the wavelength λ_1 is set as the input.

E. 2M Design of an EO Full Adder

From prior discussion, it is a fact that calculation effort is doubled due to the infeasibility of the XOR operation in processing the sum result as discussed above. It is also true that the sum calculation does not lie in the critical path which means it does not propagate to the next bit and has no influence in the total propagation latency. Therefore, realization of the sum calculation using electrical components will not violate the directed logic criteria and still keeps the optimal performance. Fortunately, it also reduces half complexity of the design because of the elimination of the $\bar{C}$ related arm. Fig. 5 shows the two-modulator (2M) design, where the optical carry signal is separated into two parts by a passive splitter. A small portion is fed into a photodetector (PD) and converted into an electrical signal which goes through an XOR gate together with P_n to get the sum signal for the current bit. The remaining part is going through a modulator that is controlled by the P_n signal before merging into combiner to generate the carry signal for the next bit. In the upper arm, continuous wave λ, which is fine-tuned to ensure the balance of light intensities at the two arms of combiners, is also injected into the system.

F. Summary and Discussion

We have proposed 6M, 4M, 3M, and 2M designs of an EO full adder based on different building blocks. The pros and cons for each design are listed in Table III. The 6M design calculates the carry signals C_n and its logic negation $\overline{C_n}$ at the same time, which could be very useful for system expansion and cascading since there is no easy and efficient way to generate the logic negation in a purely optical approach. However, it suffers from the large number of modulators that complicates the control circuits. Dual-bus modulators increase the complexity of the 4M design while it also helps to get rid of optical combiners that inevitably bring 3 dB insertion loss. The 3M design has to spend extra efforts to focus more on the phase and intensity to make the system work properly. Nevertheless, it also outstands because it requires less active modulators without the cost of adding any extra electrical logic gates into the design. The 2M design shows a simplest optical layout and is free from optical crossing, but it needs extra electrical logic gates for the sum arm.

TABLE III
PROS AND CONS OF THE PROPOSED DESIGNS

Design	Pros	Cons
6M	Calculate the logic negation simultaneously	Too many modulators
4M	No combiners	Dual-bus modulators are needed
3M	Less modulators without extra electrical gates	Need to fine-tune the phase and intensity
2M	Less modulators No crossings	Extra electrical logic gates required to calculate the sum.

TABLE IV
A COMPARISON OF VARIOUS EO MODULATORS

	MZI[37]	EAM[38]	Ring[34]	Disk[24]
Footprint (μm²)	3000×500	40×10	10×10	5×5
Wavelength (nm)	1300	1615	1550	1550
IL (dB)	7.1	4.8	2.4	1.2
ER (dB)	3.4	4.6	4	6.4
Dynamic power (fJ/bit)	450	12.8	45	1
Max. bit rate (Gb/s)	50	56	56	44
Available in foundries	yes	yes	yes	yes
Wavelength selectivity	no	no	yes	yes

IV. SELECTION OF COMPACT POWER-SAVING MODULATORS

In these proposed EO full adders, the most crucial components are the EO modulators that map signals from electrical domain into optical domain efficiently. The properties of these EO modulators directly determine the system performances, including the EO switching time, power consumption, and packing density. Therefore, a comparison of various high-speed modulators in silicon platform is carried out here.

Due to the precious space on a chip in a high-density integrated system, the device footprint is a priority. It is even more pivotal for components along the critical path since it determines the system latency which is proportional to the effective optical path. Among the variety of EO modulators used in silicon integrated photonics, as listed in Table IV, Mach-Zehnder interferometer (MZI) based modulators always have a large footprint as well as consume lots of power because of the large driving voltage and high capacitance. Generally speaking, the length of MZI-based modulators lies in the range of few hundreds of microns to millimeters, which is one to two orders of magnitude larger than other kinds of compact modulators. Surprisingly, microdisk modulators own the smallest footprint even compared to microring modulators that are well-known

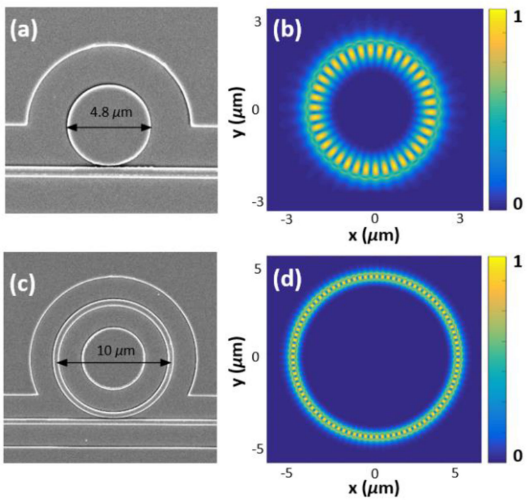

Fig. 6. SEM pictures and mode profiles of (a), (b) a fabricated microdisk with a radius of 2.5 μm and (c), (d) a microring with a radius of 5 μm.

and are most widely used nowadays. In fact, despite the similarity in shape, microrings and microdisks confine and guide light by two different mechanisms, i.e., bending waveguide mode and whispering gallery mode, respectively [30]. The former uses two physical side-walls to confine the light while the latter relies on one curved outside boundary to trigger total internal reflection. The fabricated microdisk and microring structures as well as the mode profiles are shown in Fig. 6. For microrings, a ridge near the core waveguide is always required for junction doping and electrode contacts. On the contrary, microdisks could allow p and n contacts to be fully integrated inside the disk and etch through the Si layer outside the boundary, forming a hard wall for better light confinement and eventually leading to a smaller resonator size [24], [31]. A smaller cavity will further reduce the capacitance and dynamic power consumption as well as offer a larger free spectrum range than that of microrings which may contribute to more efficient DWDM. It is a fact that the quality factor of a microdisk resonator with a radius of 1.5 μm is comparable to that of a microring resonator with a radius of 4.5 μm [24]. In practice, most of the ring modulators that have been demonstrated so far are around 10 μm in diameter [32]–[34] while disk modulators could achieve smaller than 5 μm in diameter [24], [35]. It proves to have larger than four times improvement in on-chip device packing density, which benefits the high-density device integration with advanced CMOS integrated circuits.

Most of the modulators operate at 1550 nm wavelength except electro-absorption modulators (EAM) such as germanium-on-silicon modulator due to the band-edge effects. It should be noted that some recent research has tried to use germanium silicon alloy to engineer the wavelength intentionally but at the cost of higher fabrication complexity [36]. Further, since the cutting edge of the absorption curve of an EAM is not very sharp, it will cause relatively larger insertion loss (IL) than other types of modulators, which eventually increases the power budget in a cascade system or, in other words, shortens the optical link without an amplifier.

Dynamic power consumption (power per bit) is another crucial figure of merit of an optical modulator, which is defined as the power required to switch the states (turn on/off) and is always estimated as $CV^2/4$, where C is the junction capacitance and V is the swing voltage. Therefore, reducing the capacitance and the voltage contributes to realizing a power efficient modulator. A small voltage also contributes to the integration with advanced CMOS driving circuits and eventually enables the chip-scale electronic-photonic hybrid system [39]. MZI based modulators consume lots of power due to the large size as well as the large swing voltage. For an EAM modulator, it also requires relatively large power because of the additional power transition from light to photocurrent. For the microresonator based modulators, as has been discussed above, the ultracompact size of the microdisks leads to a smaller capacitance as well as a larger overlap with the active region especially with the assistance of the vertical junction. Consequently, less voltage is required to make a considerable spectrum shift and at the same time achieve a decent modulation depth. With the reduced capacitance and voltage, the total power consumption of a microdisk to achieve an on/off switch could decrease to the sub-femtojoule region. For instance, for the microdisk modulator with record performances presented in 2014 by Timurdogan *et al.*, it consumes less than 1 fJ/bit since the capacitance and the swing voltage are only 17 fF and 0.5 V, respectively [24], which paves the way to realizing femtojoule/bit class communication links. As a comparison, for a typical microring modulator, the capacitance of the device is 30 fF and the swing voltage it needs is 2.5 V with final power consumption of 45 fJ/bit [34].

Last but not the least, all the types of modulators listed in Table IV are available in foundries, which means they have been well developed and the performances can be guaranteed. This paves the way to the future large-scale integration of optical circuits like the CMOS.

Based on the discussion above, in order to achieve a high-speed and low-power-consumption EO full adder, we choose microdisks as the EO modulators in our design due to its compactness, low insertion loss, large extinction ratio, and low power consumption.

V. Experiment

Since the 2M design owns the simplest optical circuit without any crossings or phase issues that may complicate the system, this design is adopted here for the following demonstration. Fig. 7(a) shows a 32-bit full adder which is obtained by tiling the 2M design in the horizontal as well as the vertical directions, which demonstrates a good scalability of the directed-logic-based EO full adder. As can be seen, each unit consists of two microdisks and several passive splitters and combiners. Continuous wave and carry signals will travel through every block. Fig. 7(c)–(f) show scanning electron microscope (SEM) pictures and microscope photographs of the building blocks in each full adder, including the microdisk modulator and the combiner.

Hereinafter, we choose to demonstrate a two-bit full adder as a simple example to show the feasibility and scalability of the

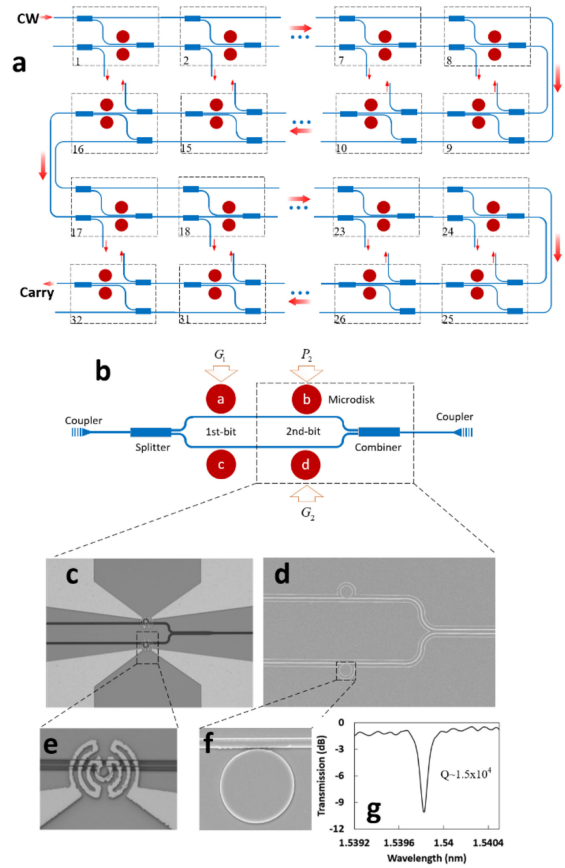

Fig. 7. Schematic diagrams of (a) a 32-bit full adder and (b) a simplified 2-bit full adder. (c), (d) Microscope photograph and SEM picture of one-bit full adder. (e) Zoom-in picture of the metallic heater. (f) Zoom-in picture of the microdisk with a radius of 2.5 μm. (g)Transmission spectrum of a single microdisk.

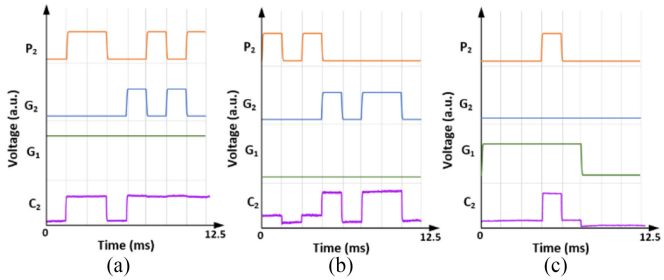

Fig. 8. Experimental results of the output C_2 with different inputs P_2, G_2, and G_1.

TABLE V
TRUTH TABLE FOR A TWO-BIT FULL ADDER

Logic inputs				Driving signals				Output
A1	B1	A2	B2	P1	G1	P2	G2	C2
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0	0
1	1	0	0	0	1	0	0	0
0	0	1	0	0	0	1	0	0
1	0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0	0
1	1	1	0	0	1	1	0	1
0	0	0	1	0	0	1	0	0
1	0	0	1	1	0	1	0	0
0	1	0	1	1	0	1	0	0
1	1	0	1	0	1	1	0	1
0	0	1	1	0	0	0	1	1
1	0	1	1	1	0	0	1	1
0	1	1	1	1	0	0	1	1
1	1	1	1	0	1	0	1	1

design. Assuming that there is no carry signal going into the first bit, i.e., $C_0 = 0$, we can easily obtain the expressions for the first two carry signals which are $C_1 = G_1\lambda$ and $C_2 = C_1P_2 + G_2\lambda$. It also illustrates that the P_1 signal along with the corresponding modulator does not play a part here. Therefore, the two-bit full adder could be redrawn as Fig. 7(b). The modulator *d* is a backup modulator. According to the schematic diagram in Fig. 7(b), the light will first be coupled into the system through a grating coupler [40] and then separate into two parts after going through a passive splitter. These two parts function as the continuous wave inputs for the first and second bit, respectively. Two light beams then get modulated by several modulators before merging into the combiner and getting coupled out of the chip through another grating coupler. The wavelength of the input light is set at the common resonant wavelength of the modulators which are originally at '0' state with '0' electrical signal input. When the electrical signals switch to '1', the transmission spectrum will redshift due to electro-refraction effect, generating a '1' optical output, as shown in Fig. 3(b). All the electrical signals G_1, P_2, and G_2 are applied into the EO modulators *a*, *b*, and *d* at the same time. The fabrication of a high-speed optical chip based on the carrier injection or depletion is extremely complicated with more than twenty masks, so we taped out our chip to the foundries and here a two-bit thermal-optic (TO) full adder based on thermal effect is fabricated and demonstrated as a proof of concept.

The TO full adder was fabricated on p-type silicon-on-insulator wafers from SOITEC with a 3 μm buried oxide layer and a thin top silicon layer of 220 nm using the nanofabrication facilities at the University of Texas at Austin. The waveguides were defined by E-beam lithography and formed by reactive ion etching. The waveguide is 450 nm in width and 220 nm in height. A separation layer of 1.5 μm SiO_2 was then deposited on the top of the waveguides, followed by the fabrication of gold microheaters and pads with a thickness of 140 nm above these microdisks. All the microdisks have radii of 2.5 μm and the gap between the mcirodisk and the waveguide is 100 nm with the quality factors of $\sim 1.5 \times 10^4$. Microscope photographs and SEM pictures are shown in Fig. 7(c)–(f). In the testing, wavelength alignment of the three microdisks was first carried out using an amplified spontaneous emission (ASE) source and an optical spectrum analyzer (OSA) before the real measurement. Then a tunable laser instead of the ASE source was used to feed light into the chip through the grating couplers and then coupled out to a photodetector followed by an oscilloscope. For the electrical signals, pseudorandom non-return-to-zero (NRZ) sequences were applied independently to these EO modulators. Fig. 8 depicts the results of the TO full adder operating at 2.56 kbs^{-1}, which turns out to be completely consistent with the truth table listed in Table V. When G_1 equals 1 in Fig. 8(a), which means the light passes the modulator *a* successfully in

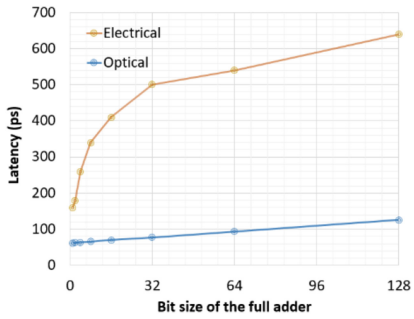

Fig. 9. Latency of electrical and optical full adder with respect to the bit size.

the first bit, the output C_2 actually becomes the logic sum of P_2 and G_2. For the other case when G_1 equals 0 in Fig. 8(b), the output shows the similar waveform with G_2 since there is no light coming through the modulators a and b in the upper arm. The reason for the multiple levels of 0 emerging in C_2 in Fig. 8(b) and (c) is that the modulators used have finite extinction ratio. Obviously, by setting a threshold, the digital signals could be obtained successfully. A modulator with larger extinction ratio could also help to alleviate this phenomenon. All the electrical parts, including the digital inputs and the sum generators, can be realized by a field-programmable gate array (FPGA), or integrated CMOS circuits [39] in the future.

VI. High-Speed Performance Projection

As one of the key active optical components in the full adder, the EO modulators mainly determine the performance of the device, including the power consumption and operation speed. As listed in Table IV, many compact high-speed modulators with low power consumption are nowadays already available even in the foundries [6], [21], [22] so that it is possible to achieve power-efficient and large-bandwidth full adders. Specifically, if we consider a full adder consisting of a microdisk with a diameter of only 10 μm along with a compact splitter and combiners [25], it only cost 0.5 ps (t_{opb}) for light to go through when the total length per bit is set at 40 μm. Therefore, under the condition that $t_{sw} = 50\,ps$ and $t_{dr} = 10\,ps$, a 64-bit full adder can still operate at a speed of over 10 GHz, as shown in Fig. 9, which is not achievable by a conventional CMOS electrical full adder [41]–[45]. In Fig. 9, we also show the simulation result of smallest latency for electrical full adders at different bit size based on a 32 nm technology library, which is the most advanced library we can have access to. In terms of the scalability, the insertion loss must be taken into consideration. The modulator itself may not cause much loss, however the combiner will intrinsically cause 3 dB loss due to the mode mismatch. Two ways to solve this problem. One is to redesign the full adder to eliminate the 3 dB loss, for example, using the 4M design shown above. Other efficient designs that we have not considered here are also possible. The other way is to use amplifiers along the path to boost the signals every several bits. We can either pump the signals using off-chip erbium-doped fiber amplifiers (EDFA) [39] or using hybrid-integrated III–V-on-silicon optical amplifiers [46]. The noise will be another concern that needs to be taken into consideration in practice since the noise will accumulate among stages. On the other hand, since sub-femtojoule athermal microdisk modulator has been realized [24], the power consumption of an EO full adder is able to be comparable with the conventional electrical full adders. But it should be noted that extra power is required to align and lock the wavelengths for resonator-based devices. There are some factors that may cause the wavelength shift. The first one is the fabrication error, which is possible to be post-trimmed [47]–[49] before use or be tuned using microheaters or DC bias without much power consumption [24]. Another one is the temperature change during operation when there is no temperature controller. A feasible way to lock the wavelength is to use feedback circuits [39], [50]. Some athermal resonator-based modulators also have been demonstrated experimentally [51], [52]. Further, in the future, it is also achievable to integrate all the components including laser sources, the amplifiers, and photodetectors in a single chip, for example, in a monolithic InP chip to further increase the system integration [53]. The chip-scale electronic-photonic fabrication technology which uses zero-change CMOS technology also makes it possible to integrate the electrical driving circuits into the system [39].

VII. Conclusion

We have proposed a new EO architecture based on the directed logic with a summary of fundamental EO logic gates so that the advantages of photonics and electronics could be full combined on a chip. Four designs of ripple-carry full adders assisted by directed logic are then proposed and discussed, which utilizes optical components to replace the conventional electrical parts in the critical path to transfer carry signals from one bit to the next. Therefore, the total latency could be largely reduced since it does not accumulate as the bit size increase. A selection of power-efficient and high-speed EO modulators is also carried out and finally a microdisk modulator is adopted due to its compactness and low power consumption. In order to demonstrate the feasibility and scalability of the proposed device, a two-bit TO full adder is fabricated and tested followed by a projection of high-speed performance with the help of state-of-the-art modulators. Further integration of photonic and electronic system remains to be explored in the future to achieve a ultracompact and power-efficient optical computing modules.

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Ray T. Chen (M'91–SM'98–F'04) received the B.S. degree in physics from the National Tsing Hua University, Hsinchu, Taiwan, in 1980, and the M.S. degree in physics and Ph.D. degree in electrical engineering from the University of California, in 1983 and 1988, respectively. He is the Keys and Joan Curry/Cullen Trust Endowed Chair with the University of Texas at Austin (UT Austin), Austin, TX, USA. He is the Director of the Nanophotonics and Optical Interconnects Research Lab, Microelectronics Research Center. He is also the Director of the AFOSR MURI-Center for Silicon Nanomembrane involving faculty from Stanford, UIUC, Rutgers, and UT Austin. In 1992, he joined the UT Austin to start the optical interconnect research program. From 1988 to 1992, he worked as a Research Scientist, Manager, and Director of the Department of Electro-Optic Engineering, Physical Optics Corporation, Torrance, CA, USA. From 2000 to 2001, he served as the CTO, founder, and Chairman of the Board of Radiant Research, Inc., where he raised 18 million dollars A-Round funding to commercialize polymer-based photonic devices involving more than 20 patents, which were acquired by Finisar in 2002, a publicly traded company in the Silicon Valley (NASDAQ:FNSR). He has been also serving as the founder and Chairman of the Board of Omega Optics Inc., Austin, TX, USA, since its initiation in 2001. Omega Optics has received more than five million dollars in research funding. His research work has been awarded more than 135 research grants and contracts from sponsors such as Army, Navy, Air Force, DARPA, MDA, NSA, NSF, DOE, EPA, NIST, NIH, NASA, the State of Texas, and private industry. The research topics are focused on four main subjects: nanophotonic passive and active devices for bio- and EM-wave sensing and interconnect applications; thin film guided-wave optical interconnection and packaging for 2-D and 3-D laser beam routing and steering; true time delay wide band phased array antenna; and 3-D printed microelectronics and photonics. Experiences garnered through these programs are pivotal elements for his research and further commercialization. His group at UT Austin has reported its research findings in more than 900 published papers, including more than 100 invited papers. He holds more than 60 patents. He has supervised and graduated 50 Ph.D. students from his research group at UT Austin. Many of them are currently professors in the major research universities in USA and abroad.

Dr. Chen has chaired or been a program-committee member for more than 120 domestic and international conferences organized by IEEE, SPIE (The International Society of Optical Engineering), OSA, and PSC. He has served as an Editor, Coeditor, or coauthor for more than 25 books. He has also served as a Consultant for various federal agencies and private companies and delivered numerous invited/plenary talks to professional societies. He is a Fellow of OSA and SPIE. He was the recipient of the 1987 UC Regent's Dissertation Fellowship and the 1999 UT Engineering Foundation Faculty Award, for his contributions in research, teaching, and services. He was the recipient of the Honorary Citizenship Award in 2003 from the Austin city council for his contribution in community service. He was also the recipient of the 2008 IEEE Teaching Award, and the 2010 IEEE HKN Loudest Professor Award, and 2013 NASA Certified Technical Achievement Award for contribution on moon surveillance conformable phased array antenna. During his undergraduate years at the National Tsing Hua University, he led the 1979 university debate team to the Championship of the Taiwan College-Cup Debate Contest.