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Low dark current III-V on silicon photodiodes by heteroepitaxy

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Abstract: Top-illuminated PIN and modified uni-traveling carrier (MUTC) photodiodes based on InGaAs/InAlAs/InP were epitaxially grown on Si templates. Photodiodes with 30-μm diameter have dark currents as low as 10 nA at 3 V corresponding to a dark current density of only 0.8 mA/cm^2. The responsivity, 3-dB bandwidth, output power and third-order output intercept point (OIP3) were 0.79 A/W, 9 GHz, 2.6 dBm and 15 dBm, respectively.

OCIS codes: (250.0250) Optoelectronics; (040.0040) Detectors.

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1. Introduction

Si has been a well-developed material in semiconductor industry for decades not only because of its abundant supply and low cost, but also its mature processing technologies. However, in order to achieve optoelectronic functionalities at telecom wavelengths, typically other materials have to be integrated on Si. For photodiodes (PDs) at 1550 nm wavelength, the material candidates include Ge and group III-V semiconductors.

However, while Ge can be grown on Si, the dark current density of Ge PDs typically ranges between 2 - 200 mA/cm^2 [1] - [5], which is higher than their III-V counterparts. In addition, since optical absorption of Ge drops significantly above 1550 nm, the low responsivity in surface-normal illuminated Ge PDs usually excludes them from usage in long wavelength applications such as dense wavelength division multiplexing (DWDM). Several Ge PDs have also been characterized at high power levels. In [6], a saturation current of 15.5 mA was achieved for a Ge-on-Si waveguide PD but only at DC. In [7], a RF saturation power of 3.7 dBm was measured for a Si/Ge UTC-PD but at a relatively low frequency of 3 GHz. In contrast, record-high RF saturation power of 12 dBm at 40 GHz was achieved for a waveguide-coupled MUTC-PD based on InGaAs/InP [8].

Integration of III-V compound semiconductors with Si photonics has drawn significant interest since it can leverage the mature Si CMOS technology to reduce manufacturing costs while exploiting III-V materials to achieve high-performance devices. There are several integration methods with hybrid integration being one of them [9], [10]. This approach involves precise alignment of discrete parts and can be considered a packaging effort rather than a true wafer-scale solution. Wafer or die bonding is another method [11], [12]. III-V wafer dies are bonded to the Si using special surface treatment or an adhesive layer. Potential drawbacks of this method are the stringent requirements on wafer surface conditions and a lower wafer throughput since the III-V

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dies are individually attached to Si.

In contrast, heteroepitaxial growth is a true wafer-level solution. Nowadays III-V epi-layers with low defect density can be grown on Si using buffer layers and annealing procedures. In addition to low dark current, the desired metrics of a PD include high responsivity, large bandwidth, high power handling capability and high linearity. In this work, PDs based on III-V materials were realized on a Si template through heteroepitaxy. We found that these PDs on Si can achieve performance similar to their counterparts on native InP substrate.

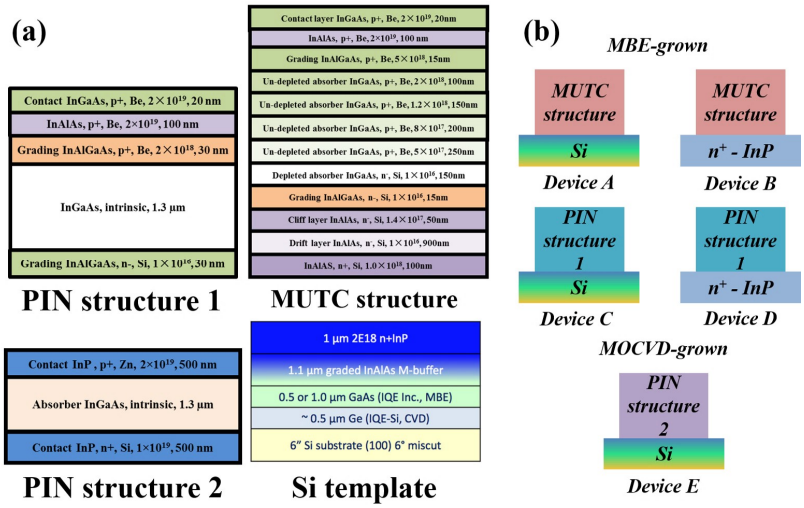

Fig. 1. (a) Epi-layer designs for PIN and MUTC PDs. (b) PD structures that were grown and fabricated.

2. Experimental

The InP-on-Si template consists of a 500 nm Ge layer, 1 μm GaAs layer, 1.1 μm InAlAs linearly graded buffer layer, and 1 μm InP virtual substrate grown by molecular beam epitaxy (MBE). Atomic force microscope (AFM) measurement showed a smooth surface morphology with a RMS roughness of 0.9 - 1.3 nm from a 5×5 μm^2 scan. Various epi-layer designs including PIN [13] and modified uni-traveling carrier (MUTC) PD [14] were then grown on top of the Si template by MBE or metal-organic chemical vapor deposition (MOCVD). The epi-layer designs and InP-on-Si template are shown in Fig. 1 (a). After the epi-growth, device C (Fig. 1 (b)) was characterized by X-ray diffraction (XRD) and AFM. The results are shown in Fig. 2. The XRD peak of InP/InGaAs epi-layers can be clearly seen and it indicates good crystallinity. The RMS surface roughness increased to 6.56 nm after epi-growth as can be seen in the optical image in Fig. 2 (b), which might correspond to the slightly broadened epi-layer XRD peak.

Five types of PDs were fabricated as shown in Fig. 1 (b). The PIN and MUTC epi-layer designs were grown on both the Si template and the n^+-InP substrate for a direct comparison. All PDs were fabricated using contact photolithography. The mesas of devices C, D and E were dry-etched while the mesas of devices A and B were wet-etched. Ring contacts were used for top illumination. The RF pads were deposited on a 2 μm-thick SU-8 layer. For the PDs on Si template, the 1-μm thick n^+-InP virtual substrate was removed in this region to minimize the pad stray capacitance. An air-bridge was used to connect the top ring contact to the RF pad. The detailed fabrication process can be found in [15]. The PD schematic and a micrograph of the

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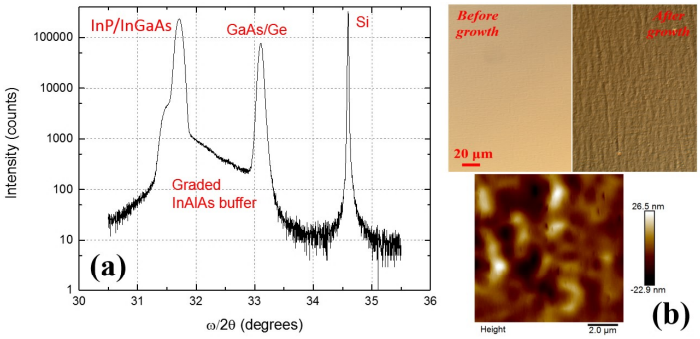

Fig. 2. (a) XRD, (b) Optical image and AFM result of device C.

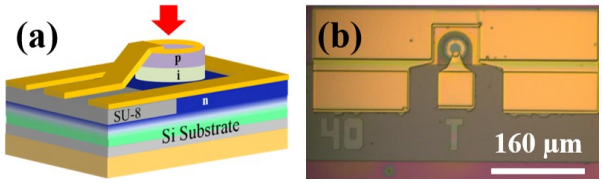

Fig. 3. (a) PD schematic. (b) Optical image of the PD.

fabricated device are shown in Fig. 3 (a) and (b), respectively.

3. Results and discussion

The dark current-voltage (I-V) characteristics of 30-μm diameter PDs were measured and the results are shown in Fig. 4. All PDs have a low dark current of less than 10 nA at -3 V. There is no difference between the PIN-PDs on Si template and InP substrate. Device B has a even lower dark current of 100 pA at -3 V. The inset of Fig. 4 shows the dark current of device C as a function of mesa diameter. The quadratic relation indicates the bulk-dominated dark current. Since device E has a high contact resistance in the forward bias region, it was neglected for further RF performance characterization.

The junction capacitances of the PDs were measured using a LCR meter and the results are shown in Fig. 5. A linear relationship can be seen as expected and the junction capacitance is close to the theoretical calculation based on the parallel plate capacitor model. We attribute the difference of around 70 fF between measured and calculated values to the RF pads and parasitic

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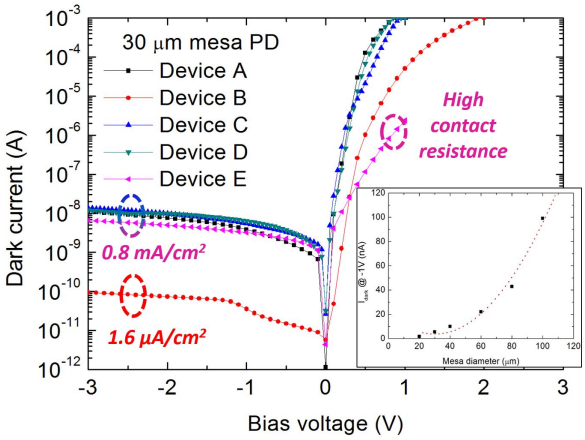

Fig. 4. Dark I-V characteristics of PDs. The inset shows the dark current of device C at -1 V bias as a function of mesa diameter. The red dotted line is a quadratic fit of the dark current at -1 V bias.

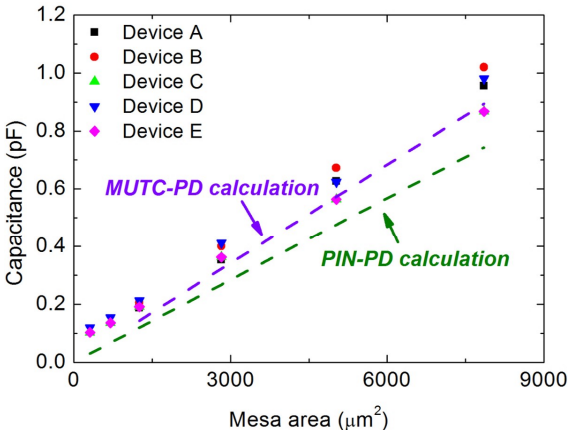

Fig. 5. Junction capacitance of PDs with different mesa area.

capacitance.

The responsivity of the PDs were measured at 1550 nm wavelength and the results are shown in Fig. 6. For device C and D, the responsivity was 0.79 A/W which agrees with our expectation. Due to the fact that there was no anti-reflection coating (ARC) on devices A and B and the ARC was not optimized for device E, the responsivity is lower for these three PDs. However, no significant difference can be observed between the PDs on Si template and InP substrate.

The S11 scattering parameters of the 30-μm PDs were measured using a vector network analyzer and the results are shown in Fig. 7 (a). A simple PD circuit model as shown in Fig. 7 (b) was used to extract the circuit elements through S11 fitting using Advanced Design System (ADS). R_s, C_j, L_s and C_{st} represent the series resistance, junction capacitance, series inductance and stray capacitance of the PD respectively. The RF pads were modeled by momentum simulation in ADS. The fitting curves are also shown in Fig. 7 (a). The extracted circuit elements are listed in table

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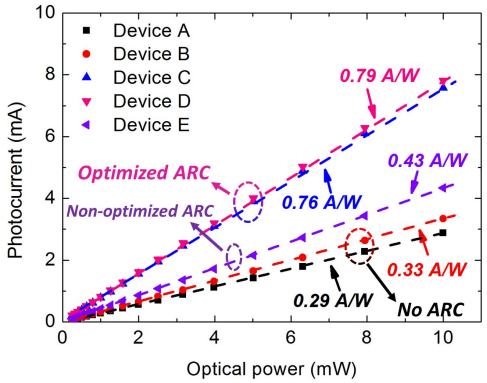

Fig. 6. PD responsivity at 1550 nm wavelength.

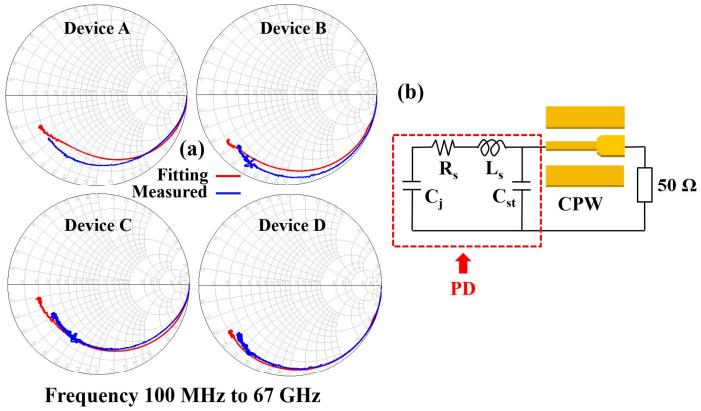

Fig. 7. (a) Measured and fitted S11 parameters of 30–μm PDs. (b) Circuit model of PDs for S11 fitting.

Table 1. **Extracted circuit elements of the 30-μm PDs**

Device	R_s (Ω)	C_j (fF)	L_s (pH)	C_{st} (fF)
A	65	104	13	80
B	80	97	18	130
C	50	100	15	79
D	25	99	8	122

1. We find that R_s has relatively high values which is most likely due to the lateral and contact resistance of the ring contact [16]. In addition, we find that the stray capacitance of devices B and D are higher than that of devices A and C. This is caused by the highly-doped InP substrate

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underneath the SU-8 stage where the RF pads were deposited on.

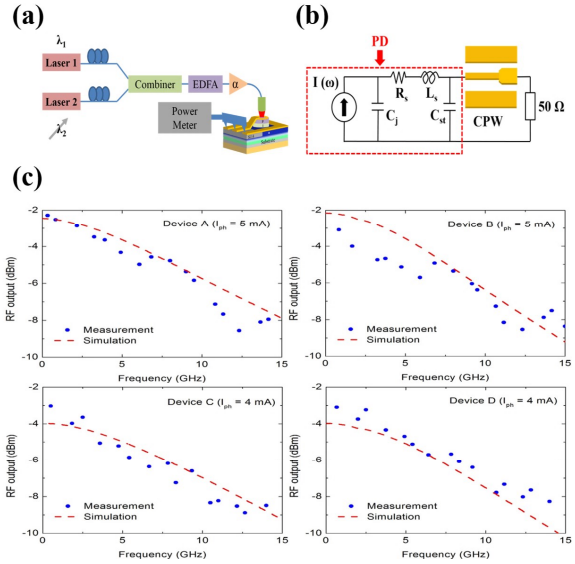

Fig. 8. (a) Optical heterodyne bandwidth measurement setup. (b) Circuit model used for bandwidth simulation. (c) Measured and simulated 3-dB bandwidth of the PDs with 30 μm diameter.

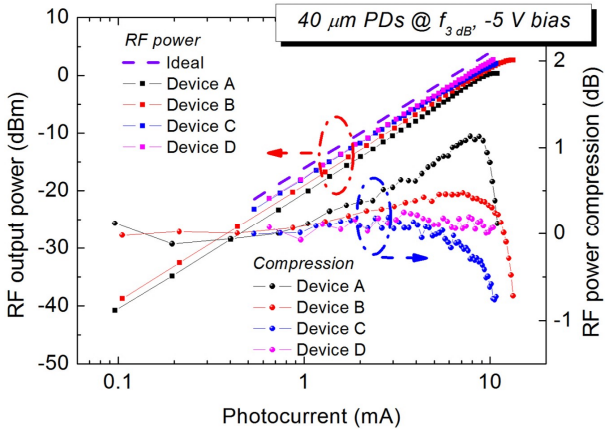

Fig. 9. RF output power and RF power compression of the PDs with 40 μm diameter.

The bandwidth of the PDs with 30 μm diameter was measured using an optical heterodyne setup shown in Fig. 8 (a). The extracted circuit model shown in Fig. 8 (b) was used to simulate the bandwidth of the PDs. The transit time effect was taken into account by the frequency-dependent current source I(ω) for MUTC-PDs and PIN-PDs according to [17] and [18], respectively. The measurement and simulation results are shown in Fig. 8 (c) for different types of PDs. The bandwidth was measured at 5 mA photocurrent for MUTC PDs and 4 mA for PIN PDs. Devices C and D show a 3-dB bandwidth of 7 GHz while devices A and B show only a slightly higher bandwidth of 9 GHz. We believe that the difference is due to the lower carrier saturation velocity of InAlAs compared to InGaAs in the depleted drift layer. Also shown in the figure are the

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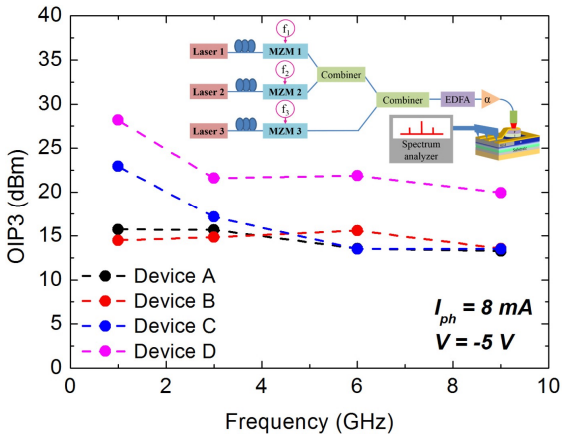

Fig. 10. OIP3 vs. frequency. The inset shows the 3-tone measurement setup.

Table 2. **Top-illuminated PDs on Si reported in the literature**

Ref.	I_{dk} (mA/cm^2)	R (A/W)	BW (GHz)	P_{sat} (dBm)
This work	0.8	0.79	9	2.6 @ 9 GHz
[20]	40	0.6	14	NA
[7]	57	0.18	10	3.7 @ 3 GHz
[21]	82	0.12	20	1.7 @ 20 GHz
[22]	20	NA	29	NA
[23]	100	0.035	39	NA
[24]	2	0.036	15	NA
[25]	100	0.07	NA	NA
[26]	1989	0.62	21.5	NA
[27]	484	0.73	12	NA
[28]	382	0.7	39	NA
[29]	6	NA	9	NA

Notes:

I_{dk}: dark current at -1 to -3 V bias voltage.

R: responsivity around 1550 nm wavelength.

BW: 3-dB bandwidth.

P_{sat}: 1-dB RF saturation power.

All references are Ge-on-Si results except for [20].

bandwidth simulation in ADS using the extracted circuit models for the PDs. The simulation results agree well with the measurements. To further increase the bandwidth, both the series resistance and the stray capacitance need to be reduced. We expect that this can be achieved by optimizing the contact resistance and using semi-insulating substrate. No difference in bandwidth was found between the PDs grown on Si template and InP substrate.

The 1-dB RF saturation power quantifies how much power a PD can deliver and it was measured

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at the 3-dB bandwidth frequency of the PDs using the optical heterodyne setup. The results are shown in Fig. 9. The 1-dB saturation photocurrents of all PDs are larger than 10 mA and the RF saturation output power can reach 2.6 dBm. Again, there is no notable difference between the PDs grown on Si template and InP substrate.

The OIP3 is an important figure of merit which quantifies the linearity of the PDs. The OIP3 of these PDs were measured using a 3-tone method [19] from 1 GHz to their 3-dB bandwidth frequency. The results are show in Fig. 10. The OIP3 for all devices is larger than 15 dBm across the frequency band. For devices A and B, their OIP3 is almost the same and frequency-independent. For devices C and D, the OIP3 decreases at higher frequency. Device D has the highest OIP3 above 20 dBm across the frequency band.

4. Conclusion

Low dark current photodiodes based on III-V materials directly grown on Si template were successfully realized. The PDs have dark currents as low as 10 nA at 3 V and responsivities as high as 0.79 A/W. The bandwidths are 7 GHz for the PIN PDs and 9 GHz for the MUTC PDs. The RF saturation power reached 2.6 dBm and the OIP3 is larger than 15 dBm over the bandwidth. The comparison of the results in this work and those in the literature is given in table 2. As can be seen, our PDs achieve the lowest dark current and highest responsivity among the top-illuminated PDs on Si reported in the literature. The fact that no significant difference in performance was found between the PDs on Si template and PDs on native InP substrate makes direct epitaxial growth of III-V materials on Si a promising approach for long-wavelength PDs on Si.

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