This paper was not presented at the conference:

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Event Name:	CLEO: QELS_Fundamental Science
Year:	2017

On-chip Microring Resonator Based Electro-optic Full Adder for Optical Computing

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Abstract: We propose a ripple-carry electro-optic full adder using microring resonators, taking advantage of unique properties of light on chip. This proposed design with larger bandwidth and lower power consumption paves the way to future optical computing.

OCIS codes: (200.4660) Optical logic; (250.3750) Optical logic devices; (130.3120) Integrated optics devices

1. Introduction

With the continuous shrinking of transistors and on-chip metal interconnects to be keeping pace with Moore's Law, the power consumption and transmission bandwidth of silicon electronics have been approaching the inevitable limits [1]. The exponentially increasing bandwidth requirements for modern computing demand a brand-new generation of alternative techniques to continue Moore's Law. Silicon photonics is believed to be one of the promising alternatives due to its potential of using unique properties of light on chip as well as compatibility with CMOS fabrication process.

Electro-optic logic gates and modules, as the building blocks of optical computing, have gained intensive attention recently because of the accessibility and maturity of abundant compact optical components, such as electro-optic modulators [2], interconnects [3] and photodetectors [4]. Various silicon based optical logic devices have been proposed and demonstrated experimentally, showing the potential for realizing future high-speed and low-power consumption optical computing [5, 6].

In this paper, we propose a new design of electro-optic (EO) full adder on SOI (silicon on insulator) platform using two silicon microring resonators (MMRs). Simulation results show that the proposed full adder using carrier injection is capable of functioning over 1Gbps with ~4dB insertion loss per bit without amplifiers in between. The experiments using thermal-optic modulation with heaters as a proof of concept will be carried out in the future.

2. Theory and design

Given the two input operands a_n, b_n and the carry from previous bit C_{n-1}, the full-adder functionality to obtain the desired outputs S_n and C_n at the nth bit can be summarized by

$$C_n = (a_n \oplus b_n)\bullet C_{n-1} + a_n \bullet b_n = p_n \bullet C_{n-1} + g_n \,,$$
$$S_n = C_n \oplus (a_n \oplus b_n) = C_n \oplus p_n \,, \tag{1}$$

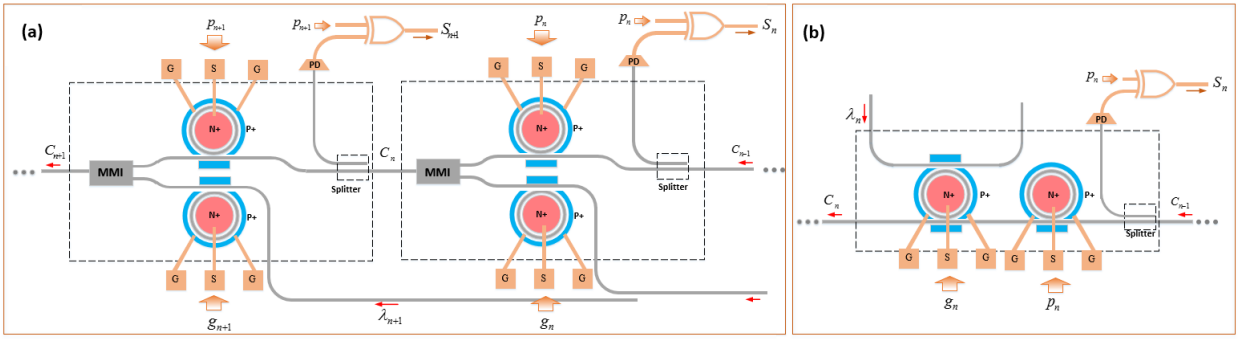

Fig. 1. Architecture of the proposed EO full adder. (a) 2-bit for parallel design, (b) 1-bit for series design. Carrier injection based modulation approach is shown here, with grey parts representing the optical waveguide and brown ones representing the electrical parts (MMI: multimode interference, PD: photodetector).

where $p_n = a_n \oplus b_n$ and $g_n = a_n \bullet b_n$. Obviously, the carry signal C is the only one that travels from one bit to the next, which intrinsically will cost a conventional electrical full adder much time to wait for the previous carry signal before proceeding to the next bit, leading to relatively large latency. In contrast, because of the much higher speed of photons on chip compared to electrons, we can process p and g signals in parallel and process the carry signal with negligible latency.

The architecture of the proposed EO full adder is shown in Fig. 1, including two different kinds of design, i.e. serial and parallel design. Here we take the parallel design as example. Driving electrical signals p_n and g_n, originating from a_n and b_n, are applied to MMRs to implant these 0/1 signals to the light passing through. The carry signal C_{n-1} from previous bit and a continuous wave λ are fed into the current one. The C_{n-1} will first split into two parts. One of them goes directly into the photodetector to generate an electrical signal and then goes through an XOR gate together with p_n and finally leads to the desired sum S_n. The other one is modulated by p and then merges into the output port through a multimode interference (MMI) coupler along with a g_n modulated λ. Finally, the optical signal C_n is obtained. The modulation method used here is carrier injection, which has been fully investigated in the past decade[2]. Modulation speed as high as 12.5 GHz with low-power consumption (~300fJ/bit) and low insertion loss (<0.5dB) has been demonstrated. In addition, the electrical modules, i.e. photodetector and XOR gates, can also be integrated in the SOI platform in the same chip[4]. The principle of the serial design is very similar but it has the advantage of lower insertion loss due to the elimination of MMI coupler which suffers from 3 dB insertion loss inevitably.

3. Result

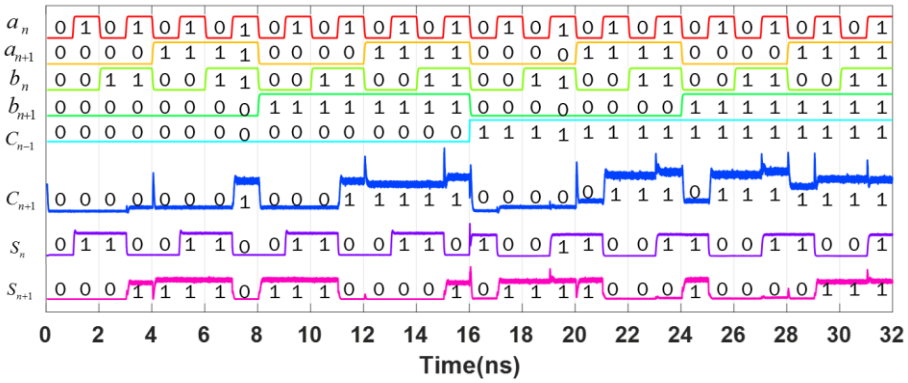

Fig. 2. Simulation results of the proposed 2-bit full adder.

In order to validate the proposed architecture, we simulate a 2-bit full adder of the parallel design (Fig. 1(a)) with a bit rate at 1GHz. All parameters in the simulation are set using experimental data from publications. It turns out that the simulation results show great consistency with the ones in the truth table which is not listed here. One can find that all 32 desired logic states have been realized, as shown in Fig. 2.

In conclusion, we have proposed an architecture of EO full adder on the SOI platform, and validated it through numerical simulation of a 2-bit case of the parallel design. This study paves the way to future high-speed and low-power consumption optical computing.

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The authors acknowledge the Multidisciplinary University Research Initiative (MURI) program through the Air Force Office of Scientific Research (AFOSR), contract No.FA 9550-17-1-0071 , monitored by Dr. Gernot S. Pomrenke.