Optical switches based carry-ripple adder for future high-speed and low-power consumption optical computing

Zheng Wang[§ 1, 2], Zhoufeng Ying[§ 2], Shounak Dhar[§ 2], Zheng Zhao[§ 2], David Z. Pan[2], and Ray T. Chen[1, 2, 3]

[§]These authors contributed equally to this work

[1]Materials Science and Engineering Program, Texas Materials Institute, The University of Texas at Austin, Austin, Texas 78712, USA

[2]Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78712, USA

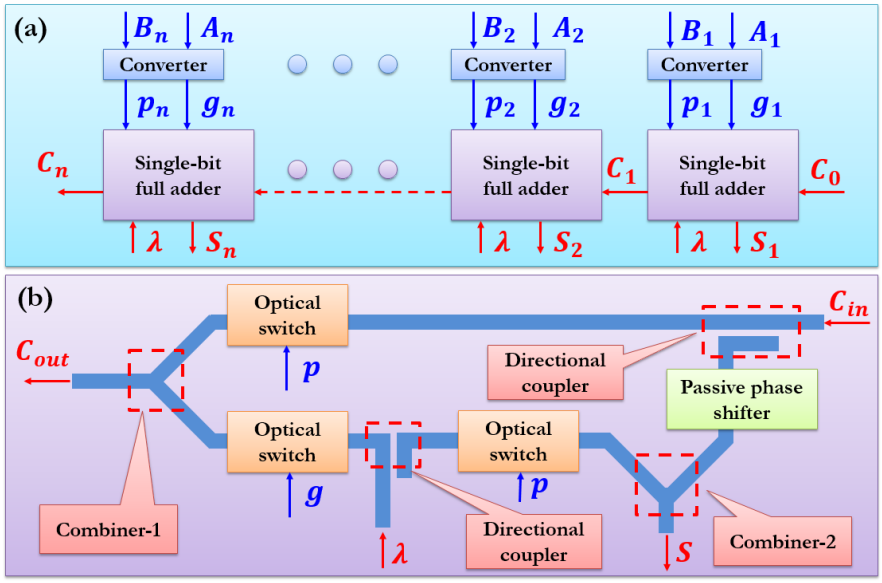
[3]Department of Mechanical Engineering, The University of Texas at Austin, Austin, Texas 78712, USA

Author e-mail address: (wangzheng@utexas.edu, dpan@ece.utexas.edu, chenrt@austin.utexas.edu)

Abstract: We report an optical switch based architecture for realizing optical computing. Numerical simulation has been performed to validate the architecture by adopting CMOS compatible PN depletion micro-ring resonator as the approach for optical switching.

OCIS codes: (200.0200) Optics in computing (200.3760) Logic-based optical processing (200.4660) Optical logic

Due to ever increasing demand for information bandwidth, and with electronics approaching their performance limit, there has been a renewed interest in using optical logic for computing and signal processing over the past decade [1,2]. System advantages that the optical schemes promise over the conventional electronic schemes include: (1)significant reduction of gate latency (enabling complex logic operations beyond 10GHz), (2)ultra-low energy consumption per bit (energy is not expended during the process of computing, the logic levels 0 and 1 are treated as input signal for modulation, and it is only expended when the final result is being extracted [3]), and (3)simplified layout architecture for many complex computation structures. For example, full adder is a fundamental operation for computation. However, a conventional carry-ripple adder will be too slow for many-bit addition due to excessive carry propagation delay though it has a concise layout. Modern microprocessors all have to use complicated adder structures such as parallel prefix adders to obtain satisfactory performance while they come with inevitable power penalty [4,5]. The greater the number of bits, the more complicated and power hungry the adder will become. In this paper, we propose an optical switch based architecture of carry-ripple adder, which utilizes the specific merit of light that interference, for future high-speed and low-power consumption optical computing. The proposed architecture of carry-ripple adder is shown in Fig.1 (a) and its key component that single-bit full adder is illustrated in Fig.1 (b).



(c)

Inputs			Driving		Outputs	
A	B	C_{in}	p	g	C_{out}	S
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	1	0	0	1
0	1	1	1	0	1	0
1	0	0	1	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	1	0
1	1	1	0	1	1	1

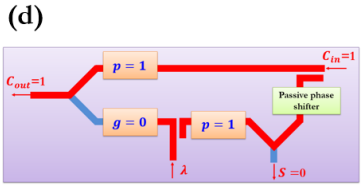
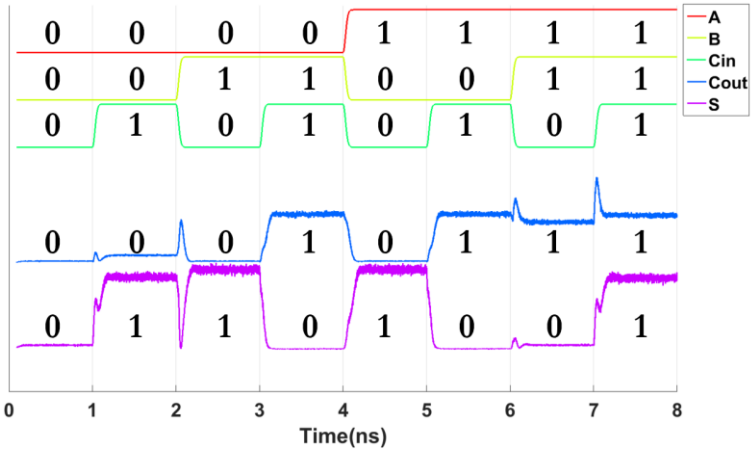


Fig. 1 (a) Proposed architecture of carry-ripple adder (b) Schematic of a single-bit full adder (c) Truth table of a single-bit full adder (d) A single-bit full adder working at the input status that $A = 1$, $B = 0$, and $C_{in} = 1$

In our architecture, the input signals A_n and B_n will first be converted to p_n ($P_n = A_n$ XOR B_n) and g_n ($g_n = A_n$ AND B_n). Then p_n and g_n will serve as the driving signals of a single-bit full adder (SBFA) to control its optical switches. When the driving signals represent logic *0*, the optical switches will be at off-state and drop the light away. When the driving signals represent logic *1*, the optical switch will be at on-state and light could pass. Each SBFA needs

three driving signal inputs (two p and one g) to perform the addition operation and then output two optical signals C_{out} and S. To realize the addition operation by interference between two optical signals, besides the optical signal that C_{in} from the previous SBFA, another CW laser which is coherent with C_{in} at the selected working wavelength λ needs to be fed into the full adder. At the combiner-1 in our SBFA, the optical signals C_{out} will be generated by the interference between p_n modulated C_{in} and g_n. To generate the optical signals S at the combiner-2, a constant phase shift needs to be added to assure the two optical signals have π phase difference before the interference happening in the combiner-2. By defining that the high-intensity level of the optical signals as logic *1* while the low-intensity level as logic *0*, one could realize the desired truth table which is shown in Fig.1(c). To illustrate the working principle of our SBFA, we take the input status that $A = 1$, $B = 0$, and $C_{in} = 1$ as an example. For this input status, the corresponding driving signals are $p = 0$ and $g = 1$. For the two input arms of the combiner-1, only the upper arm will have light ($p = 1$, light could pass) as the optical switch at the lower arm would drop the light away ($g = 0$). At the combiner-2, though light exists in both arms, the π phase difference will result in a destructive interference, and the output signal has a low-intensity level. A schematic of the SBFA working at this input status is shown in Fig.1 (d), the light exists (high-intensity level) in the red waveguides while not in the blue waveguides (low-intensity level).

In principle, our architecture for optical carry-ripple adder does not limit the approach for optical switches. One could select any approach among thermo-optical (TO), electro-optical (EO), acousto-optical (AO), optical-optical (OO) and etc. However, considering the state-of-the-art manufacturing technologies mastered till now, an EO hybrid architecture by utilizing complementary metal–oxide–semiconductor (CMOS) manufacturing technology is the most economically attractive solution. In the EO hybrid architecture, the converters will be realized by electronic logic gates, and then the electrical driving signals will be applied to EO switches. As the light propagation delay between each SBFA is much smaller than that in equivalent electrical circuits, the electronic signals could be computed in parallel for all bits. For an n-bit carry-ripple adder, our EO hybrid approach could reduce the total latency from to $T = (n\text{-}1) \times (T_{XOR} + T_{AND} + T_{OR})$ to $T \sim \mathrm{Max}[T_{XOR}, T_{AND}]$. Here we have selected PN depletion micro-ring resonators [6] as the implementation of EO switches to validate our architecture. The simulated results of an SBFA working at 1 Gb/s are shown in Fig.2, one could easily see that all desired logic operations have been realized.



Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Fig. 2 Simulated dynamic operation results of an SBFA at the speed of 1 Gbps via PN depletion micro-ring resonators based EO switches.

In conclusion, we propose an optical switch based architecture of a carry-ripple full adder and validated the architecture via numerical simulation. This study is essential towards achieving the holy grail of high-speed and low-energy optical computing.

Reference

[1] Xu, Qianfan, and Richard Soref. "Reconfigurable optical directed-logic circuits using microresonator-based optical switches," Opt. Express **19**, 5244-5259 (2011)

[2] Soref, Richard. "Reconfigurable integrated optoelectronics," Advances in Optoelectronics 2011 (2011)

[3] Hardy, James, and Joseph Shamir. "Optics inspired logic architecture," Opt. Express 15, 150-165 (2007)

[4] Roy, Subhendu, et al. "Towards optimal performance-area trade-off in adders by synthesis of parallel prefix structures," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. **33**, 1517-1530 (2014)

[5] Roy, Subhendu, et al. "Polynomial time algorithm for area and power efficient adder synthesis in high-performance designs," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst **35**, 820-831 (2016)

[6] Dong, Po, et al. "Low V pp, ultralow-energy, compact, high-speed silicon electro-optic modulator," Opt. Express **17**, 22484-22490 (2009)

The authors acknowledge the Multidisciplinary University Research Initiative (MURI) program through the Air Force Office of Scientific Research (AFOSR), contract no. FA 9550-17-1-0071, monitored by Dr. Gernot S. Pomrenke